REMARKS

Claims 5 and 8-10 are allowed; claims 1-4 are rejected; and claims 6-7 and 11-22 are withdrawn from consideration as being directed to a non-elected invention.

Review and reconsideration on the merits are requested.

First, because claim 5, which is an independent claim, is allowed, Applicants respectfully request the Examiner to withdraw the restriction requirement with respect to claims 6 and 7 depending from and including all of the limitations of allowed claim 5.

Claims 1 and 2 have been amended to recite that the plurality of electrically conductive vias all have a straight shape. Support is found, for example, as shown in Fig. 2 where capacitor 31 has a plurality of electrically conductive vias 35, penetrating the capacitor main body between upper surface 32 and lower surface 33 and connected to surface-connecting terminals 36, 37.

Claims 3 and 4 have been amended to recite that the plurality of electrically conductive vias all have a straight shape, and to further require a thermal expansion coefficient of the capacitor main body that is smaller than that of the substrate. Support is found, for example, at page 10, lines 29-32 of the specification.

Claims 11-22 directed to a non-elected invention have been canceled. Applicants reserve the right to file a divisional application directed to the canceled subject matter.

New claims 23-26 correspond to claims 1-4 as originally filed, respectively, except that these claims further require a capacitor main body having a first ceramic surface (on which a semiconductor device having surface-connecting terminals is to be mounted).

Turning to the cited prior art, claims 1-4 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,775,150 to Chakravorty et al. Chakravorty et al. was cited as disclosing a capacitor and assembly meeting the terms of the rejected claims.

Applicants traverse, and respectfully request the Examiner to reconsider in view of the amendment to the claims and the following remarks.

Fig. 3 of Chakravorty et al. cited by the Examiner illustrates a cross-section of the die/substrate structure of Fig. 2, where the multilayer substrate comprises an organic portion 80 and a ceramic portion 90. Ceramic portion 90 includes an embedded capacitor comprising an insulating layer of high permittivity material arranged between plates 141 and 151 (column 4, lines 39-48 and column 5, lines 18-24 of Chakravorty et al.). In Chakravorty et al., organic portion 80 is provided for routing and fanning out of conductor traces for I/O signals (column 4, lines 49-52).

In response, claims 1-4 have been amended so as to include the feature "the plurality of electrically conductive vias all having a straight shape". In contrast, some of the vias in Chakravorty et al. have bent portions. This feature of amended claims 1-4 shortens the wiring for connection between the semiconductor device and the substrate, as shown in the drawings of the present specification.

The straight shape is further desirable for the following reasons.

(1) The straight shape is advantageous from a manufacturing process point of view since all of the via holes can be formed at one time and all of the vias can be formed by filling

via paste in all the via holes at one time. In contrast, the capacitor of Chakravorty et al. requires every layer of every divided and stacked unit of layers to have independently formed vias.

(2) The straight shape enables vias made of metal having good thermal conductivity to provide a good and efficient heat radiation effect (so-called thermal via effect). The good heat radiation effect of the capacitor that is disposed adjacent the semiconductor device can effectively suppress or restrain a temperature rise of the semiconductor device in use, and can lower the thermal load on the wired substrate made of a resinous material having a low heat resistance.

Further, claims 3 and 4 have also been amended to include the feature "the thermal expansion coefficient of the capacitor main body being smaller than that of the substrate". This feature of amended claims 3-4 is effective for reducing thermal stress on the semiconductor device.

Because amended claims 1-4 differ from Chakravorty et al. with respect to one or more elements thereof, claims 1-4 are not anticipated by Chakravorty et al. Additionally, the significance of the plurality of electrically conductive vias all having a straight shape (claims 1-4) and as further requiring a thermal expansion coefficient of the capacitor main body that is smaller than that of the substrate (claims 3 and 4) has been discussed above. For these additional reasons, it is respectfully submitted that amended claims 1-4 are also patentable over Chakravorty et al.

Withdrawal of the foregoing rejection under 35 U.S.C. § 102(e) is respectfully requested.

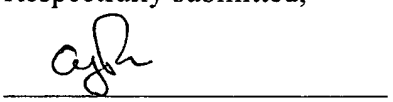
New claims 23-26 characterize the capacitor as having an approximately plate-shaped capacitor main body having a first ceramic surface and a second surface, so as to exclude substrate 50 of Chakravorty et al. including organic portion 80 from the scope of the claimed "plate-shaped capacitor main body." As such, the assembly of Chakravorty et al. comprising organic portion 80 at a top surface does not meet the subject limitation of new claims 23-26. For example, Fig. 3 of Chakravorty et al. does not meet claim 23 requiring a plate-shaped capacitor main body having a first ceramic surface on which a semiconductor device is to be mounted.

Withdrawal of the rejection over Chakravorty et al., withdrawal of the restriction requirement with respect to claims 6 and 7 and allowance of claims 1-10 and 23-26 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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